A Report on

DC-DC POWER CONVERTER RESEARCH

FOR ORBITER/STATION POWER EXCHANGE

submitted to

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I. Executive Summary

A. Background

This project was to produce innovative DC-DC power converter concepts which are appropriate for the power exchange between the orbiter and the Space Station Freedom (SSF). The new converters must interface three regulated power buses on SSF, which are at different voltages, with three fuel cell power buses on the orbiter which can be at different voltages and should be tracked independently. Power exchange is to be bi-directional between the SSF and the orbiter. The new converters must satisfy the above operational requirements with better weight, volume, efficiency and reliability than is available from the present conventional technology. Two families of zero current dc-dc converters were developed and successfully adapted to this applications. Most of the converters developed are new and are presented in this report for the first time.

The features of the desired power exchange interfaces can be described in two parts: the Assembly Power Converter Unit (APCU) and the NSTS Power Converter Unit (NPCU). The APCU, which is shown in Figure 1, is a dc-dc power converter which interfaces the 28 VDC orbiter power buses with the 120 VDC and 130 VDC power buses of the space station. This converter is to be used during the initial space station assembly, when no station power is generated, to transfer power from the orbiter to the station. There are three independent fuel cell power sources on board the orbiter. Each individual fuel cell voltage may be anywhere from 27-32 VDC and must be tracked seperately by the APCU. These three individual fuel cell power buses must deliver power

to the two station power buses in parallel, for maximum load sharing and reliability. Furthermore, the two station power buses must be regulated at 120 VDC and 130 VDC. In addition, the orbiter and the station power systems must be galvanically isolated from each other for system reliability and security reasons. The total power capability of the APCU is taken to be no less than 7.5 KW. This assigns a nominal 2.5 KW to each fuel cell but can be changed depending on the individual fuel cell voltages.

The NPCU is a dc-dc power converter which converts the 160 VDC space station power to the 28 VDC orbiter power. This unit is used, after the station contruction is completed, to extend the docking time of the orbiter during utilization flights. Here again, the individual fuel cell voltages may be anywhere from 27-32 VDC and must be individually tracked. Galvanic isolation is also required for this power converter. Total nominal power capability is to be no less than 7.5 KW in the NPCU. A block diagram of the NPCU is shown in Figure 2.

B. Report Summary

The isolated capacitor coupled converter (C^3) is proposed for the APCU and NPCU applications. The basic operation of the C^3 has been presented in a previous report to NASA Johnson Space Center. With zero current soft switching, the switching losses can be eliminated while keeping the conduction losses comparable to the conventional hard switching converter. Moreover, the C^3 operates with one switch in series with the voltage source and the load in order to reduce the on state voltage drop of the switches. Therefore, the theoretical system efficiency can be increased to 96 %. These features make the C^3 a good candidate for the orbiter and space station power exchange units.

On the other hand, the inverse dual converter (IDC) has been shown suitable for the high voltage high power applications. However, a low voltage variation of the IDC can be adapted for this low voltage aerospace power exchange application. The low voltage output is connected in series with one rectifier switch at a time. With the zero current switching to eliminate switching losses, the low voltage IDC circuit is especially suitable for the NPCU system, with a theoretical efficiency of 98 %. The study has produced a theoretical analysis and simulation result of this low voltage IDC.

This report summarizes the result of the research and development on these two zero current soft switching converters: the isolated C^3 and the low voltage IDC.

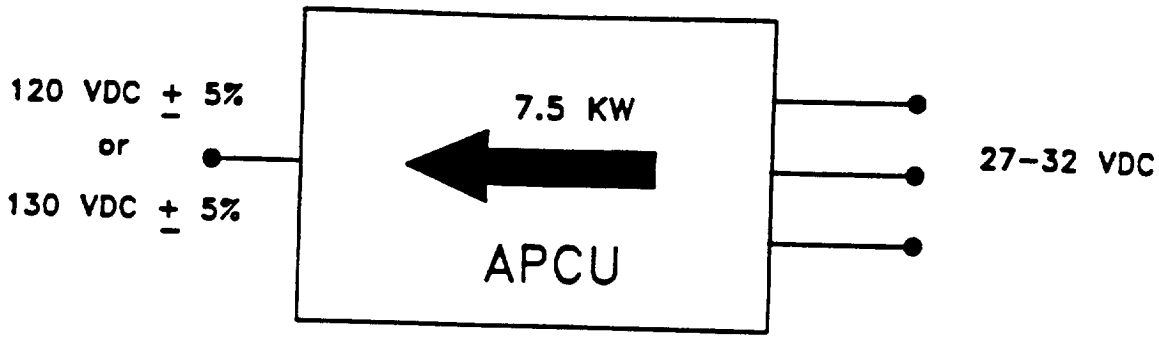


Figure 1. APCU block diagram.

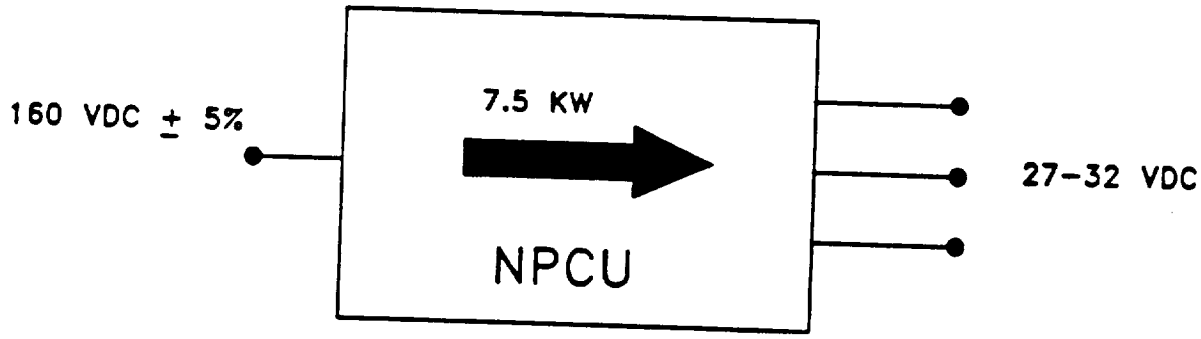


Figure 2. NPCU block diagram.

II. Soft Switched Converters

A. Soft Switching Concepts

The conventional pulse width modulation (PWM) dc-dc converter is a matured technique at low power applications with a moderate efficiency, high voltage or current stresses, and the electromagnetic interference (EMI) problem. The high switch stresses are due to the parasitic reactive components in the circuit, such as switch output capacitances, stray inductances, and the leakage inductances of the isolation transformer. Whenever a switch is turned on or off from a stiff voltage bus or a current source, these parasitic components cause a very high dv/dt or di/dt stress. Therefore, a snubber circuit is neccessary to prevent these switch stresses and increase the complexity of the converter circuit.

The solution for the EMI problem is to operate the converter at a higher switching frequency. Hence, with a high switching frequency the component size can be reduced and the power density raised. However, the switching losses of the PWM dc-dc converter have been shown to be proportional to the switching frequency. This makes the conventional PWM converters not suitable for high efficiency high power applications.

The soft switching method [1,2,3] can utilize these parasitic components to shape the switch waveforms at either zero voltage or current conditions while keeping a favorable conduction loss compared to the conventional PWM dc-dc converter. Because of the soft switching, the switching losses can be minimized and the converters can operate at a higher switching frequency. Therefore, the efficiency of the soft switched converter can be increased. This is a very

important factor for the strict aerospace power conversion applications. In the space power exchange units, the converters must satisfy higher system efficiency, better weight and higher power density.

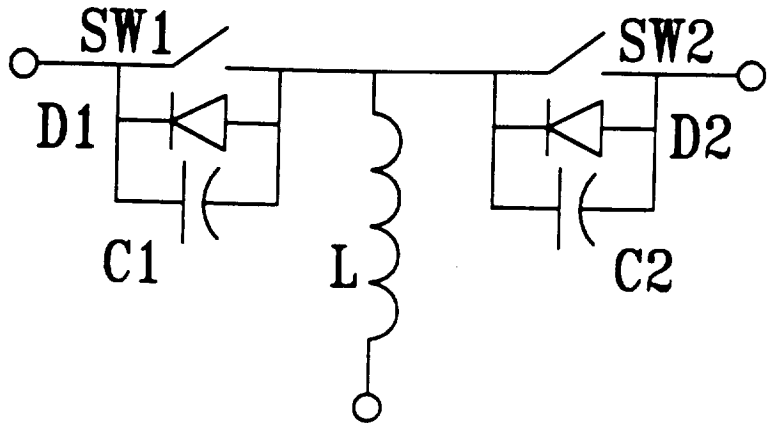
There are two types of the soft switched dc-dc converters: the zero voltage switching (ZVS) converters and the zero current switching (ZCS) converters.

A.1. Zero Voltage Switching

In a minority carrier device, such as IGBTs and power transistors, the parasitic capacitance in the semiconductor junction dumps charges into the main switch during turn-on time [3] and causes additional switching losses. One generic solution is to fully utilize the parasitic capacitance and transfer the energy stored in this capacitor to an inductor with a resonant operation in order to turn on the main switch at a zero voltage condition.

The zero voltage switch pair is illustrated in Figure 3. Zero voltage switching is achieved by transferring parasitic charges between the two output capacitors, with resonance, and clamping the switch voltage at zero by an anti-parallel diode to turn on the main switch. The parasitic capacitors also operate as lossless snubbers when the switches are turned off. Hence, there are no turn-on and turn-off switching losses dissipated in the switches with the zero voltage switching.

Some fringing voltage waveforms have been observed [4] when switches are off. These fringing effects are due to the free oscillation between the parasitic capacitor and the linked inductor after turning off the switch. It is difficult to avoid this free oscillation phenomenon which is a disadvantage of the zero voltage switching.



QS-ZV SWITCH PAIRS

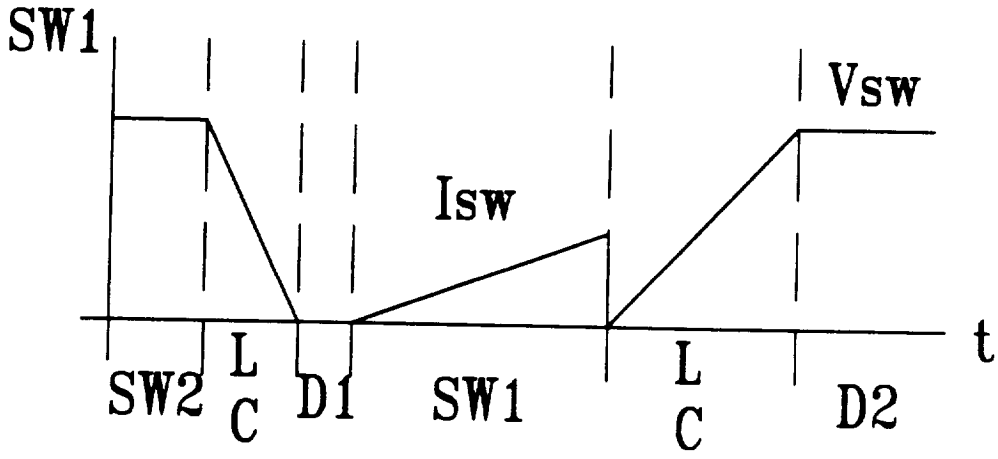


Figure 3. Zero voltage switching pair.

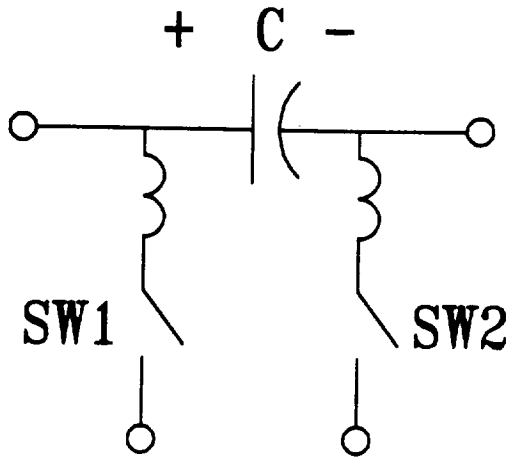
A.2. Zero Current Switching

The π model switch cell shown in Figure 4 is a quasi-square-wave zero current switch pair. Each switch is connected in series with an inductor. The coupled capacitor can form a close resonant loop with these two inductors in order to create a zero current condition for the main switch.

The zero current turn-on of the switch can be easily accomplished by the inductive snubber. To turn off a switch, the oppsite one should be turned on first. A resonant operation gradually takes the energy away from the out-going inductor and turns off the switch at a zero current condition. The switching losses can be eliminated by this energy reset mechanisim [1]. Note that instead of the dead time control, which is commonly required for the conventional PWM converter and the ZVS converter, an overlapped duration between two switches is necessary to achieve the zero current switching.

If an isolation transformer is available in the ZCS converter circuit, the leakage inductance of the transformer can perform the snubber operation by series resonance with the coupled capacitor. Therefore, no additional inductive snubbers should be in series with the main switches. This minimizes the component numbers and decreases the volume of the system.

This zero current switching pair was invented by this PI and a family of the new ZCS dc-dc converters can be based on it. Two of them, which are the ZCS C^3 and the IDC circuit, have been proposed for the APCU and NPCU power units and will be described in the following chapters.



QS-ZC SWITCH PAIRS

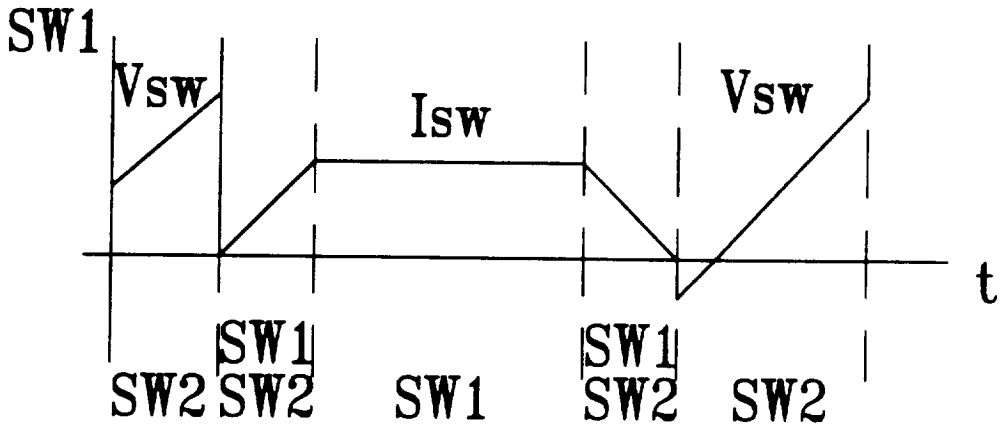


Figure 4. Zero current switching pair.

C. ZVS Converters

By inserting the zero voltage switch pair into the three basic dc-dc converter topologies; buck, boost and buck/boost converters, a family of zero voltage switching (ZVS) converters can be found as shown in Figure 5, 6 and 7. They are the ZVS buck converter, the ZVS boost converter, and the ZVS inductor coupled converter (IC^2) [5], respectively. In these converter topologies, the main switches always turn on and off with zero voltage conditions to eliminate switching losses.

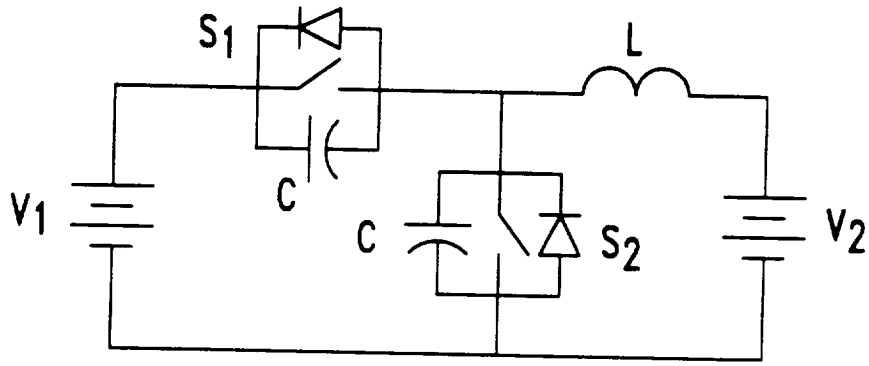


Figure 5. ZVS buck converter.

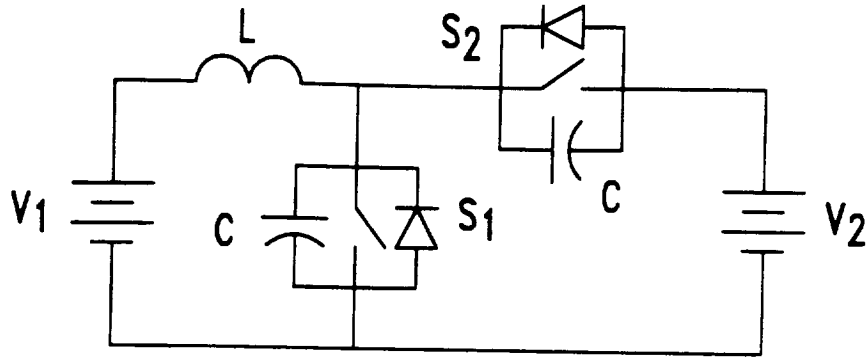


Figure 6. ZVS boost converter.

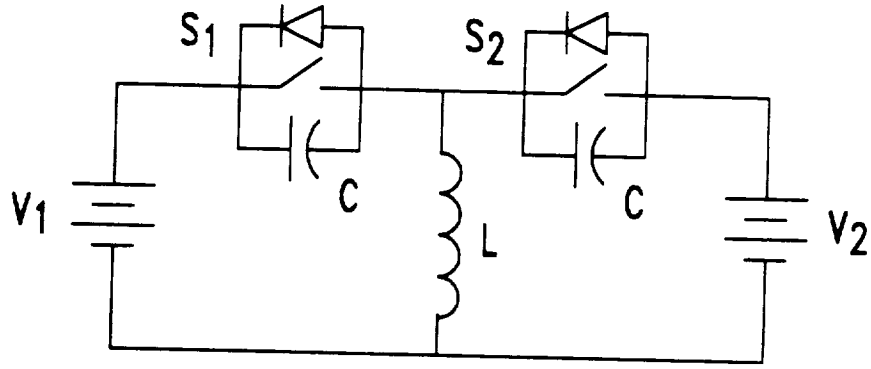


Figure 7. ZVS inductor coupled converter.

D. ZCS Converters

The duals of the ZVS dc-dc converters produce the ZCS, as illustrated in Figure 8, 9 and 10. Belonging to the family of the zero current switching (ZCS) converters are the ZCS buck, the ZCS boost and the ZCS capacitor coupled converters (C^3) [6.7]. These converters are supplied by current sources and feed into current sink loads. Some variations of these ZCS converters are presented for aerospace power exchange interfaces. The isolated C^3 circuit is derived from the basic ZCS C^3 and the low voltage inverse dual converter (IDC) is from the ZCS buck converter.

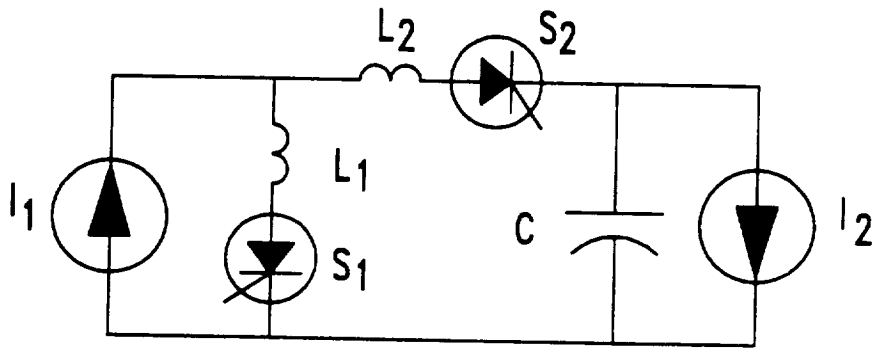


Figure 8. ZCS buck converter.

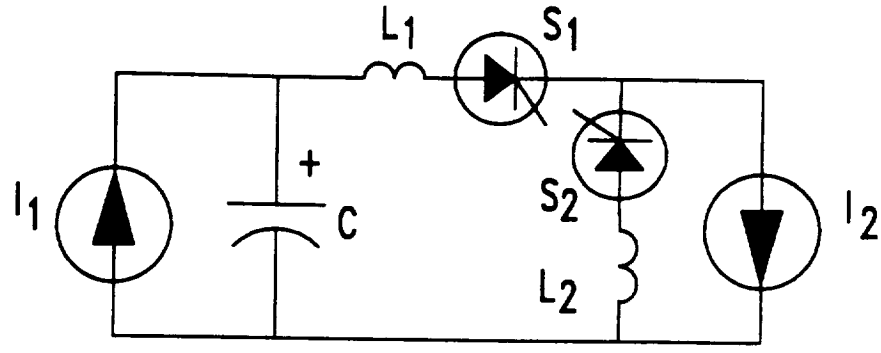


Figure 9. ZCS boost converter.

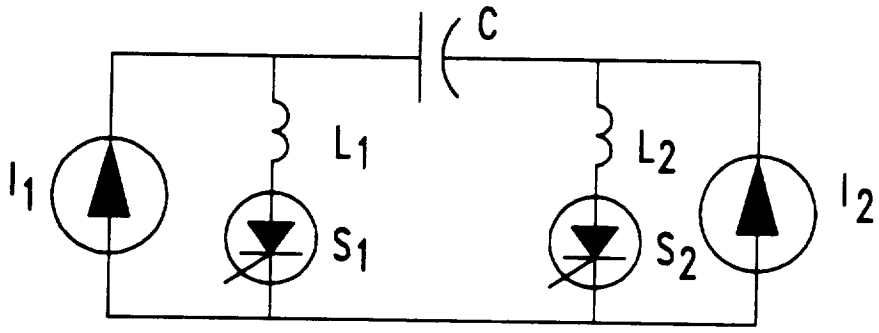


Figure 10. ZCS capacitor coupled converter.

III. Capacitor Coupled Converter

A. Circuit Description

The capacitor coupled converter or C^3 [1,6,7] was invented by this PI, at Texas A&M University, Power Electronics Laboratory. This converter is capable of soft switching. It has been shown [6] that the current stresses on the main switches of this converter remain the same as in the conventional hard switching converters while the switching losses are eliminated because of the zero current switching operation.

A low power variation of this C^3 circuit which uses a high frequency transistor for S_1 and a diode for S_2 has also been presented under the name Cuk converter [8]. However, the hard switching operation of the switch S_1 in the Cuk converter makes it inappropriate for high power applications. On the contrary, the C^3 operates with zero current switching and the switches are commutated capacitively. As previously mentioned, the switching losses are eliminated by the zero current switching operation. The heat dissipated in the switch is minimized and the life time and reliability of the power switches can be enhanced. Therefore, high power devices, such as SCRs, GTOs, and MCTs can be used and the power capability of the C^3 converter will be expanded by an order of magnitude.

The symmetrical topology of the C^3 converter makes it a bilateral power converter and the regenerated load power can be transferred back to the source. The C^3 is also capable of step-up and step-down of the output voltage, by voltage amplitude control. These features make the capacitor coupled converter particularly suitable for the aerospace power conversion applications.

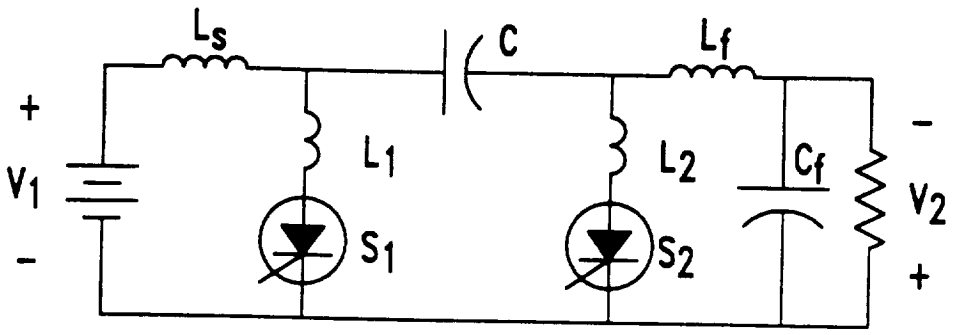


Figure 11. The capacitor coupled converter.

B. Principle of Operation

Assuming continous conduction in the source and load inductors, the capacitor coupled converter can be represented by a current source and a current sink respectively. Then, the coupled capacitor is charged by the source current I_s and discharged by the load current I_d alternatively, as shown in Fig. 12. The power switches S_1 and S_2 are connected in series with the snubber inductors L_1 and L_2 and the switching operations can be described as follows.

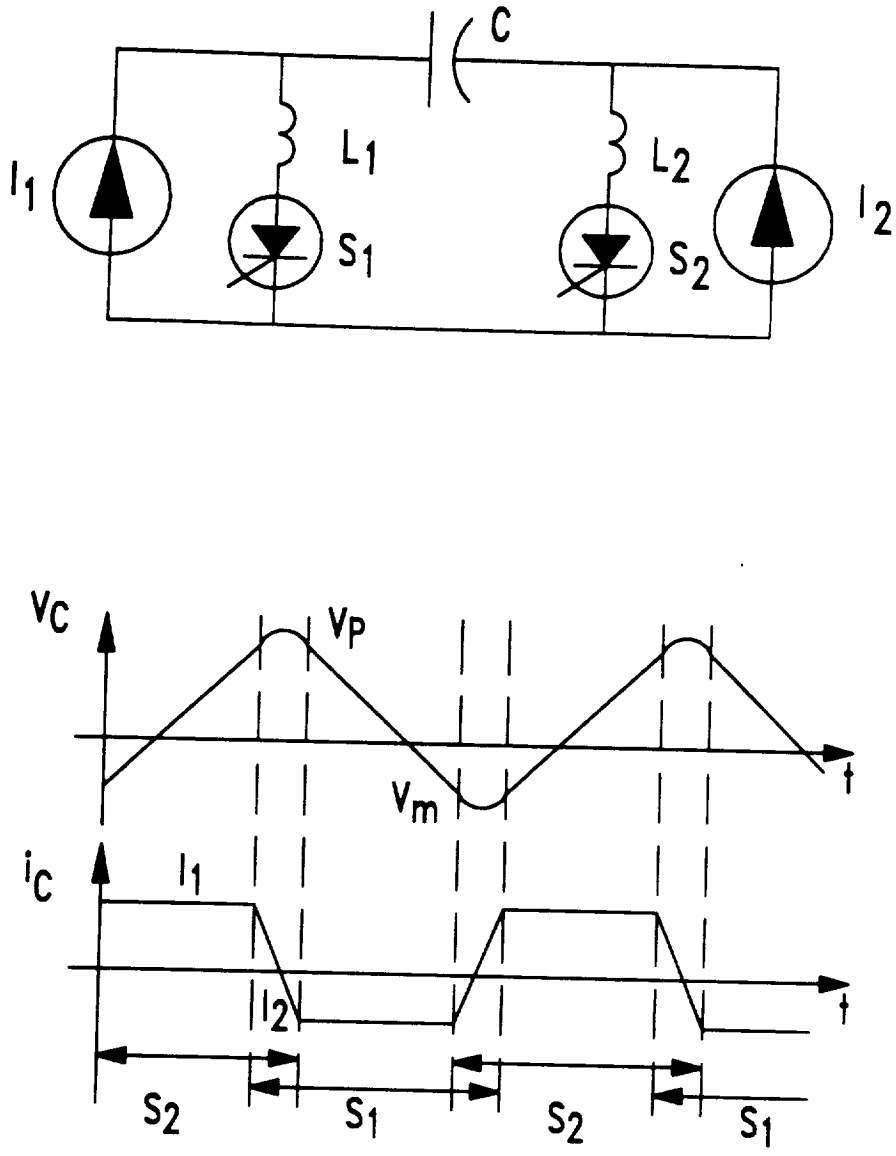


Figure 12. (a). Simplified C^3.

(b). Capacitor waveforms.

B.1. Charging Stage

The switch S_2 is on at $t = t_0$. The inductive snubber L_2 ensures S_2 to switch at zero current condition. The capacitor is charged by the current source I_s and the rising slope of the capacitor voltage is a function of the capacitance C and the current I_1. The capacitor voltage is controlled by amplitude modulation and bounded by V_p and V_m respectively, as shown in Figure 12(b).

B.2. Resonant Stage

In order to turn off S_2, the switch S_1 must be turned on at $t = t_1$. A resonant loop is then formed by the coupled capacitor and the two series inductors L_1 and L_2. The trapped inductive energy in L_2 is transferred to L_1 such that the switch S_1 is turned on at zero current while S_2 is off with the zero current switching. Note that the voltage on S_2 is reverse biased by the coupled capacitor. Therefore, the switches implemented in this C^3 circuit must be capable of reverse voltage blocking and the thyristor switches are especially suitable for this circuit.

B.3. Discharging Stage

The switch S_1 is on during $[t_2, t_3]$ and the capacitor is discharged by the load current I_2. To turn off S_1, the capacitor voltage should be able to reverse bias S_1 and turn on the switch S_2 to reset the inductive energy stored in L_1 and start the next resonance.

Note that the inductive energy is not disspated and the recirculation of this energy is achieved by an appropriate gating of the implemented switches.

Unlike the dead time control of the conventional hard switching converters, an overlapped duration between the two switches of the C^3 is necessary to ensure the zero current switching.

C. Circuit Analysis

If the resonant period is negligible and the C^3 is in the steady state operation, the inductor voltage waveforms v_{L_s} and v_{L_f}, as shown in Figure 13, have to satisfy the volt-sec balance constraints over one switching cycle.

$$\begin{aligned} \int_0^T v_{L_s}(t)dt &= 0 \\ \int_0^T v_{L_f}(t)dt &= 0 \end{aligned} \tag{1}$$

These two constraints can also be solved as follows.

$$V_1 = \frac{V_p - V_m}{2} D \tag{2}$$

$$V_2 = \frac{V_p - V_m}{2} (1 - D) \tag{3}$$

where D is the duty cycle of the switch S_1, and V_p, V_m are the positive and negative peak magnitudes of the capacitor voltage respectively.

For a steady state dc operation, the dc gain of the C^3 can be derived from the above equations and is identical to the Cuk converter.

$$\frac{V_2}{V_1} = \frac{1-D}{D} \tag{4}$$

and for energy conservation constraint,

$$\frac{I_2}{I_1} = \frac{D}{1-D}. \tag{5}$$

Moreover, the rate of energy transferred by the coupled capacitor must be equal to the rate of the energy consumed by the load R.

$$\frac{1}{2}CV_p^2 - \frac{1}{2}CV_m^2 = \frac{V_2^2}{R}T \tag{6}$$

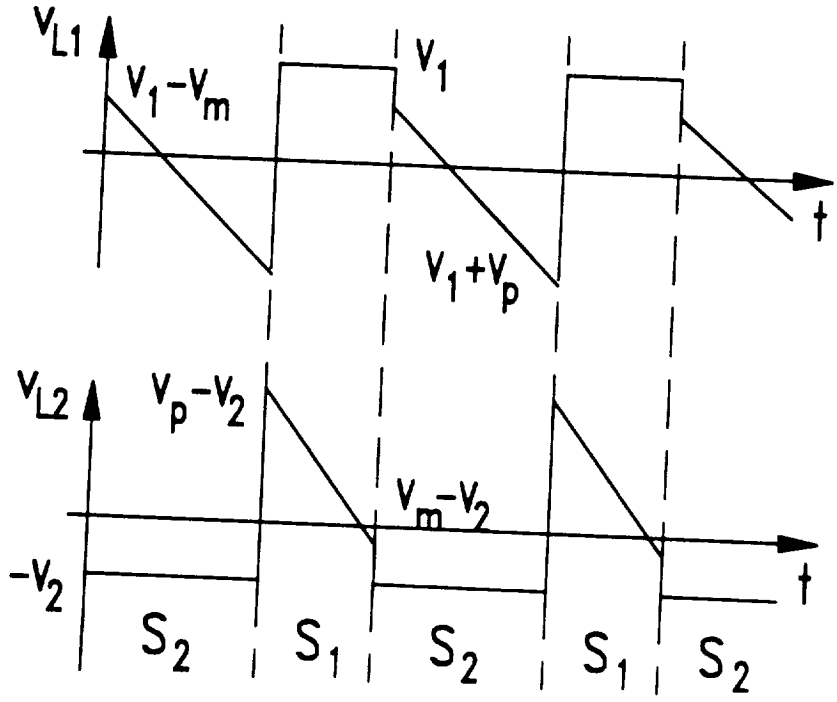


Figure 13. inductor waveforms.

where T is the switching period. If G denotes the dc gain of the C^3 converter, the equations (2), (3) and (6) can be rewritten as follows.

$$V_1 = \frac{V_p + V_m}{2}\left(\frac{1}{1-G}\right) \tag{7}$$

$$V_2 = \frac{V_p + V_m}{2}\left(\frac{G}{1-G}\right) \tag{8}$$

$$\frac{2RC}{T} = \left[\frac{G}{1-G}\right]^2 \left[\frac{V_p + V_m}{V_p - V_m}\right] \tag{9}$$

It is obvious that the dc gain G can be controlled by the magnitudes of the capacitor voltage, which are V_p and V_m. V_m can be kept constant to ensure the reverse bias commutation of the main switches and V_p is changed to accomodate the new gain. The boundary values of the capacitor voltage can be found from (7)-(9) as follows.

$$V_p = \frac{V_2}{D} - \frac{DTV_2}{2CR} \tag{10}$$

$$V_m = \frac{V_2}{D} - \frac{DTV_2}{2CR} \tag{11}$$

The capacitor voltage, according to (10) and (11), consists of a dc term, which is dependent on the load, and an alternating term representing a large ripple waveform.

As stated earlier, the dc output voltage can be controlled by the magnitudes of the capacitor voltage. Supposing the negative voltage V_m is at the minimum level in order to reverse bias the switch and the input voltage is constant, the

regulation of the dc output voltage V_2 is a function of V_p. The dynamic change in the dc output is proportional to the change of the peak capacitor voltage. By linearizing equations (11) and (12) and assuming a constant V_m, the control equation for the output voltage is found as follows.

$$\Delta V_p = \frac{DT\Delta V_2}{CR} \tag{12}$$

where ΔV_p and ΔV_2 are the changes of the peak capacitor voltage and the output voltage respectively. However, the above equation is valid only when the isolated C^3 operates below the rated power. In oder to control the output voltage, V_p is adjusted according to the above equation while the resistance R is invariant. If the dc output is varied because of a sudden change in the load, the control constraint can be determined by the following formula.

$$\frac{\Delta V_2}{V_2} = -\frac{\Delta R}{R}\cdot\frac{D^2T}{2CR - D^2T} \tag{13}$$

$$\Delta V_p = \frac{2\Delta V_2}{D} \tag{14}$$

An increase in the load causes a decreased voltage at the output, as shown in the equation (13). Therefore, equation (13) can be used to calculate the output voltage regulation from no load to full load. The corresponding change of V_p can be also found from (14).

D. Switch Realization

As previously mentioned, the main switches of the C^3 are reverse biased by the coupled capacitor C, and the circulation of the inductive energy guarantees

the zero current turn-off. This turn-off process eliminates the tailing effect, commonly found in the high power semiconductor switches, such as GTOs and IGBTs. The tailing current contributes to additional switching losses in these power switches. With the zero current switching, the high power gate turn-off switches, GTOs, IGBTs and MCTs, as well as the high current thyristor SCRs can be used in the C^3 circuit.

However, the switches of the C^3 must be reverse biased by the coupled capacitor. Therefore, a series blocking diode is necessary if implemented with IGBTs and MCTs which are not capable of reverse voltage blocking.

E. Topological Variations of C^3

Since the galvanic isolation and multibuses are required in both the APCU and NPCU realizations, the capacitor coupled converter can be modified to satisfy these requirements.

E.1. Isolated C^3

The isolated version of the C^3 circuit is illustrated in Figure 14(a). The isolation transformer is used to interface the input source with the dc load. The coupled capacitor in the C^3 has been split into two: one at the front end and one at the secondary side of the isolation transformer. These two split capacitors can improve the reliability and security of the isolated C^3 converter while performing the same function as the C^3 circuit.

The leakage inductance L_r of the isolated transformer, as shown in Figure 14 (b), can resonate in series with the coupled capacitor and two indutive snubbers during the resonant stage, and prolong the transition periods for the zero current switching of the main switches. The reverse recovery current in the thyristor switches and the tailing current in the gate-turn-off devices are dependent on the turn-off slope of the switches. Therefore, the transition duration for the zero current turn-off should be long enough to neutralize these reverse recovery charges and to ensure the next turn-on of the switches. In this sense, the isolated C^3 can take advantage of the leakage inductance in the isolation transformer. Moreover, the two inductive snubbers can be substituted by the leakage inductor in a loosely coupled transformer in order to optimize the system.

The control of the isolated C^3 circuit is the same as the basic C^3 and already described in the previuos section. With the zero current switching to eliminate the switching losses and the step-up and step down of the output voltage, the isolated C^3 is suitable for the APCU and NPCU systems.

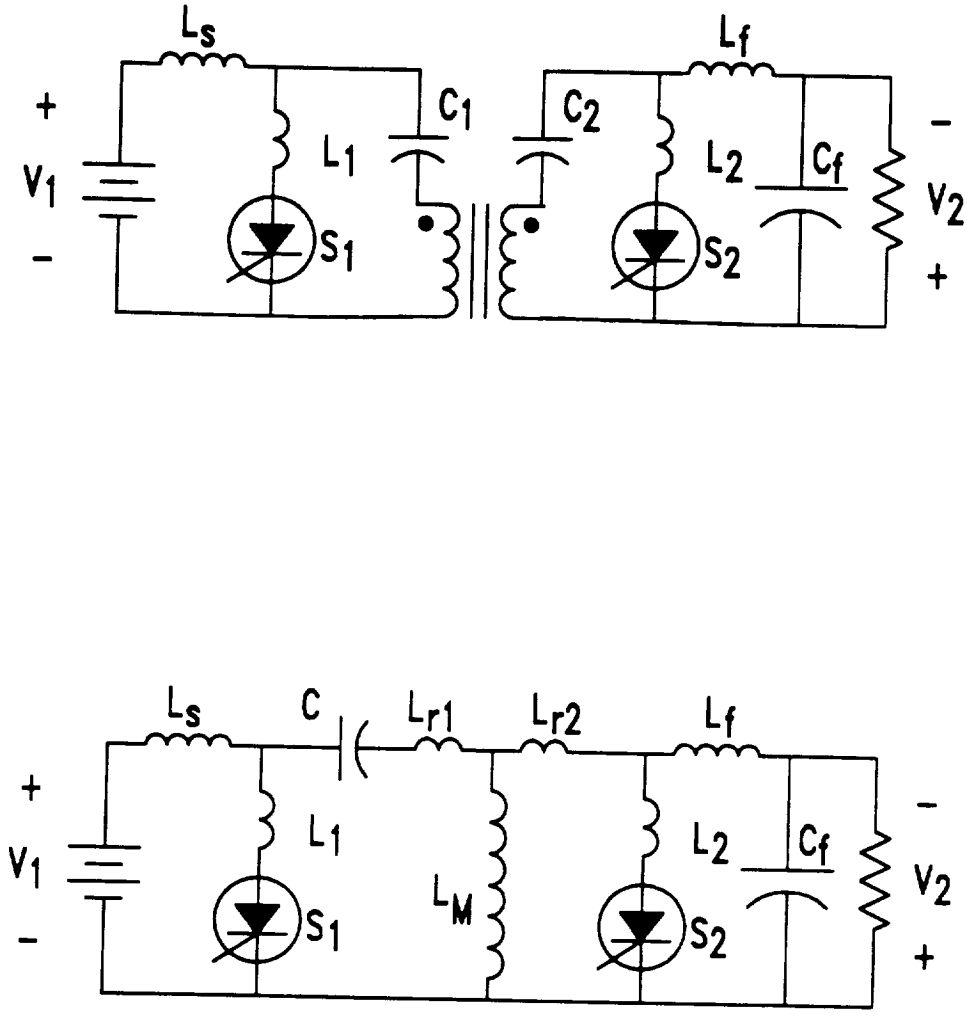


Figure 14. (a) The isolated C^3.

(b) The equivalent circuit.

E.2. Multibus C^3

The multibus C^3 circuit, as shown in Figure 15, has three different regulated dc outputs. Each dc output voltage can be tracked independently by controlling the voltage amplitude of the corresponding coupled capacitor. The operating principle of the multibuses C^3 is the same as those of the isolated C^3, with the ZCS in order to achieve a higher system efficiency.

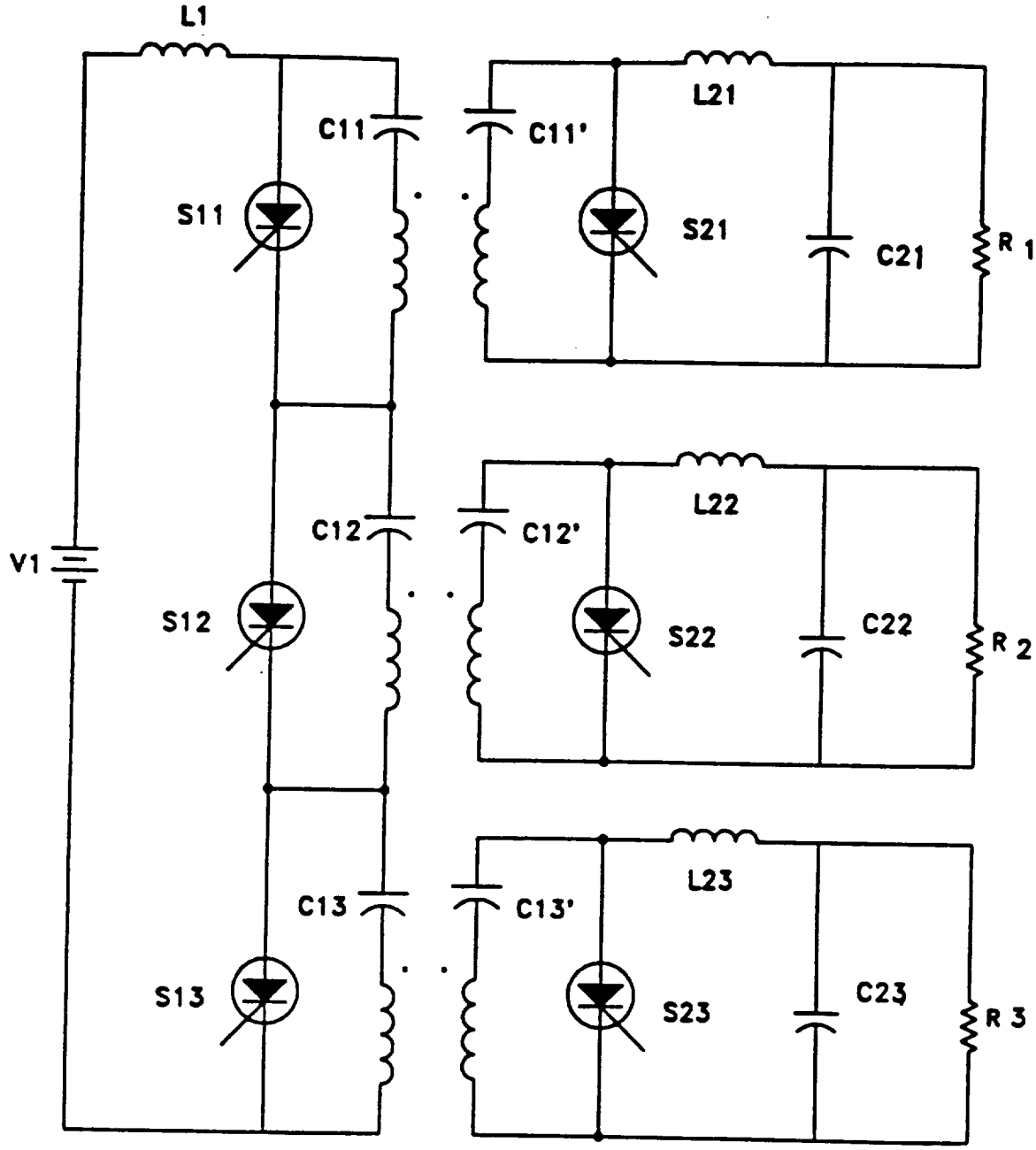


Figure 15. The multibus C^3.

F. Design Example

A design example of the capacitor coupled converter for the Assembly Power Converter Unit (APCU) will be presented for illustration. The system specifications are as follows.

Input voltage,	$V_1 = 28$ VDC
Output voltage,	$V_2 = 130$ VDC
Output power,	$P_d = 2.5$ KW
Switching frequency,	$f_s = 10$ kHz
DC gain,	$G = 4.643$

The load resistance R is

$$R = \frac{V_2^2}{P_d} = \frac{130^2}{2500} = 6.76\Omega. \tag{15}$$

The positive and negative peak voltages of the coupled capacitor, V_p and V_m can be found from equation (10) and (11).

$$\begin{aligned} V_p &= 367.1V \\ V_m &= -51.1V \end{aligned}$$

The ac coupled capacitance can be calculated from equation (9).

$$\begin{aligned} C &= \frac{T}{2R}\left(\frac{G}{1+G}\right)^2\left(\frac{V_p + V_m}{V_p - V_m}\right) \\ &= \frac{10^{-4}}{2 \times 6.76}\left(\frac{4.643}{5.643}\right)^2\left(\frac{367.1 - 51.1}{367.1 + 51.1}\right) \end{aligned}$$

$$= 3.784\mu F$$

The source and load inductors L_s and L_f can be caculated by the following approximate formulas.

$$L_s = \frac{(V_p - V_1)^2 T}{2\Delta I_s (V_p - V_m)} \left(\frac{1}{1+G}\right) \tag{16}$$

$$L_f = \frac{(V_p - V_2)^2 T}{2\Delta I_d (V_p - V_m)} \left(\frac{G}{1+G}\right) \tag{17}$$

For 20 % input and output ripple currents, $L_s = 0.028mH$ and $L_f = 2.78mH$. Similarly, the output capacitance C_f can be found from

$$C_f = \frac{\Delta I_d T}{8\Delta V_2} \tag{18}$$

where ΔV_2 is the given peak-to-peak output voltage ripple. For the APCU system, the output voltage should be regulated within the 5 % range. Therefore, the output capacitance is $C_f = 7.4\mu F$.

The basic design values are summarized in Table 1.

Table 1

C^3 design values for APCU

C	L_s	L_f	C_f	f_s
3.784 μF	.028 mH	2.78 mH	7.4 μF	10 kHz
V_1	V_2	P_d	V_p	V_m
28 VDC	130 VDC	2.5 KW	367 V	-51.1 V

G. Efficiency Calculation

The capacitor coupled converter is operated with zero current soft switching in order to eliminate the switching losses of the main switches. Hence, the overall system efficiency is expected to be higher than that of the conventional hard switching converter.

To calculate the efficiency of the C^3, two other losses should be taken into account. They are the conduction losses of the switches and the stray losses of the passive and reactive components. Since the stray losses are much smaller compared to the conduction losses, only the former will be included in the efficiency calculation.

If the C^3 is considered for the APCU system and all the specifications are the same as stated in section F, the average input and output currents can be found as I_s = 89.29 A and I_d = 19.23 A at 2.5 KW power level, respectively. Each switch, S_1 or S_2, has to carry both the currents during the on state. Assuming an 1V drop when the swich turns on, then the average conduction loss can be calculated as follows.

$$P_{cond.} = (89.29 - 19.23) \times 1 = 108.52 \text{ W}$$

The theoretical system efficiency can be found from the following cacula-tion.

$$\eta = (1 - \frac{P_{loss}}{P_{in}}) \times 100\%$$

$$= (1 - \frac{108.52}{2500}) \times 100\% = 95.57\%$$

H. Simulation and Experimental Results

Figure 16 shows the simulation results of the C^3 circuit.

Figure 17 illustrates the effect of the leakage inductance on the isolated C^3 circuit.

Figure 18 is the experimental results of the C^3 operation.

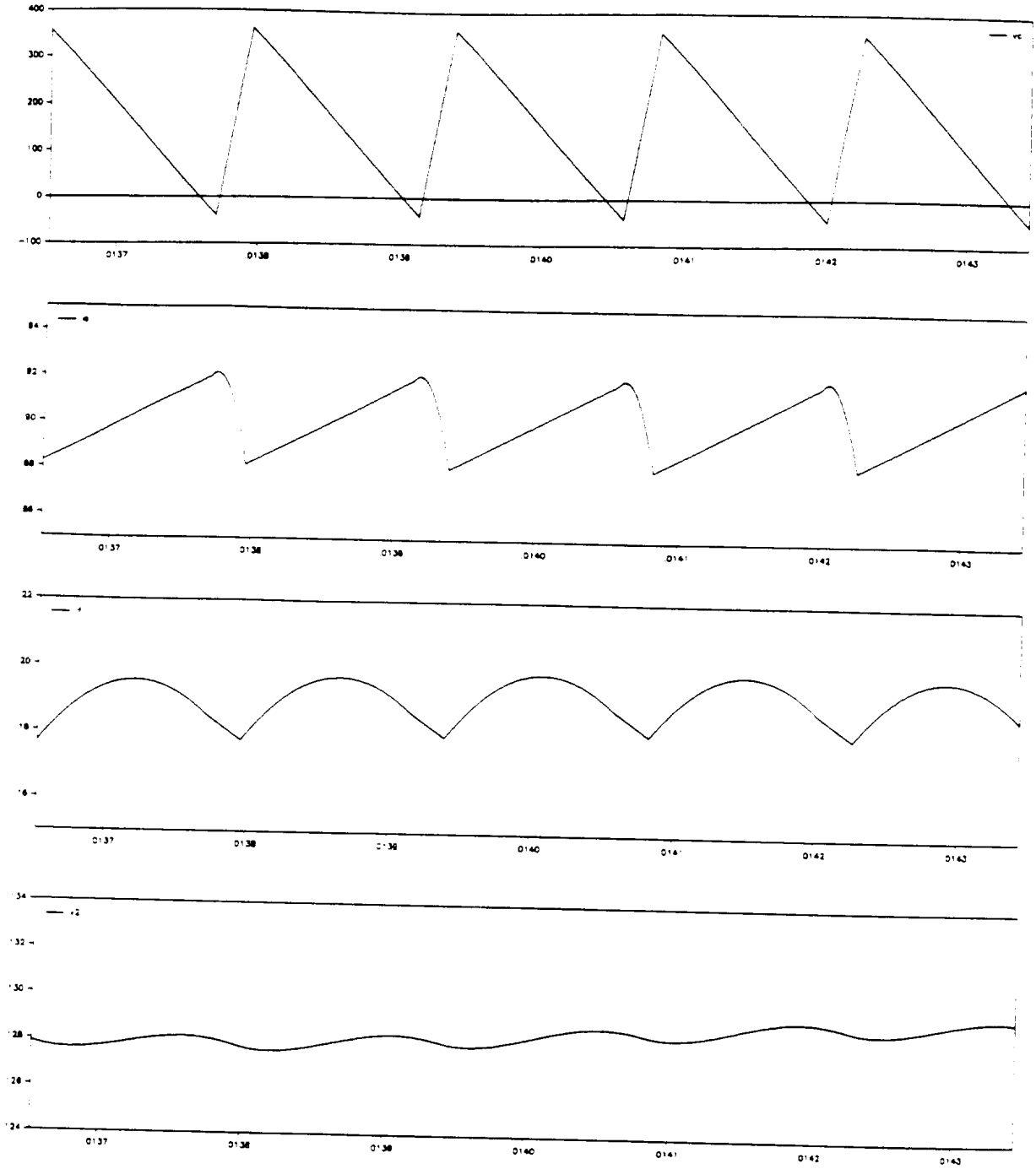


Figure 16. The simulation results of the C^3.
From the top, they are coupled capacitor voltage, input current, output inductor current and output voltage.

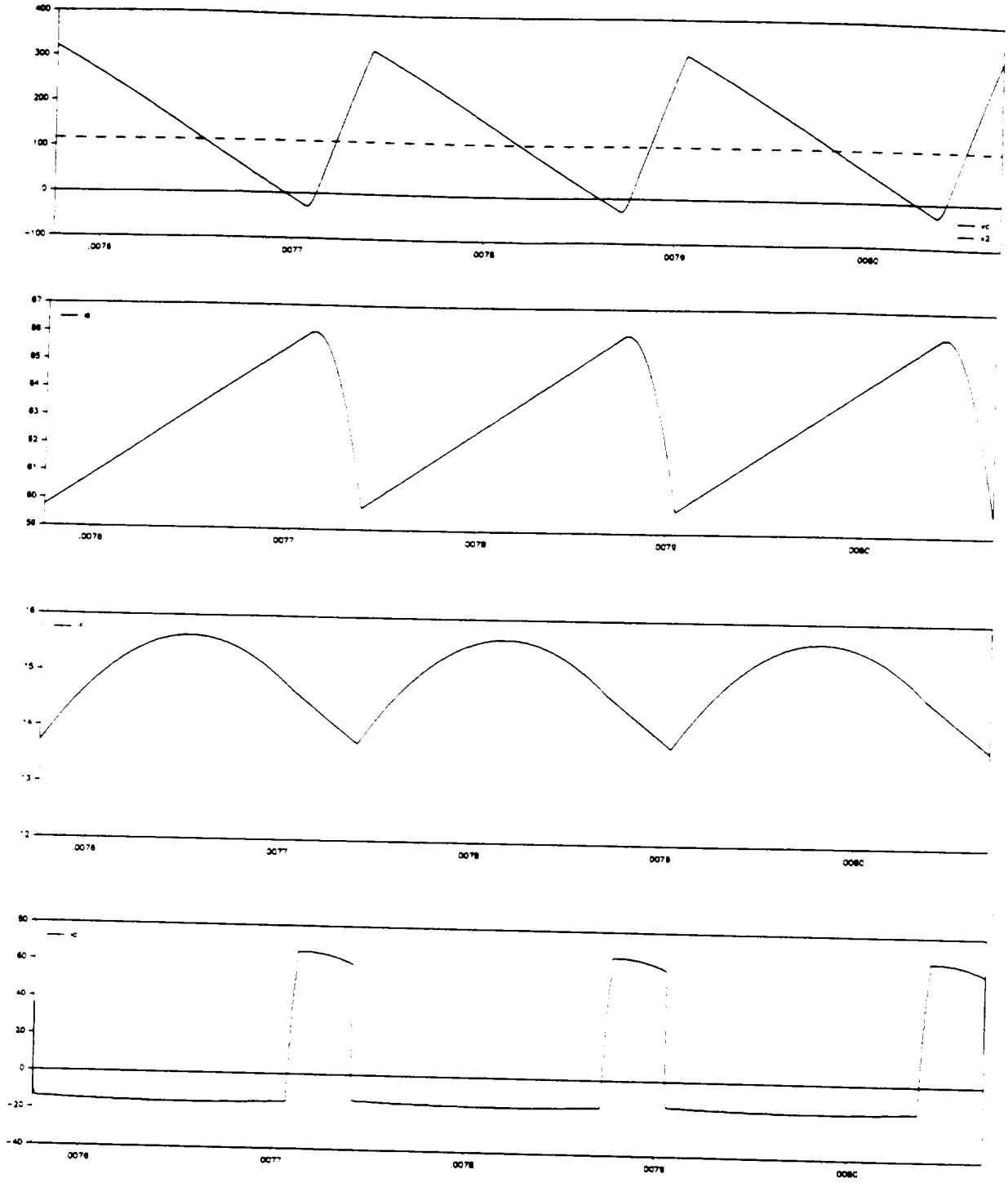
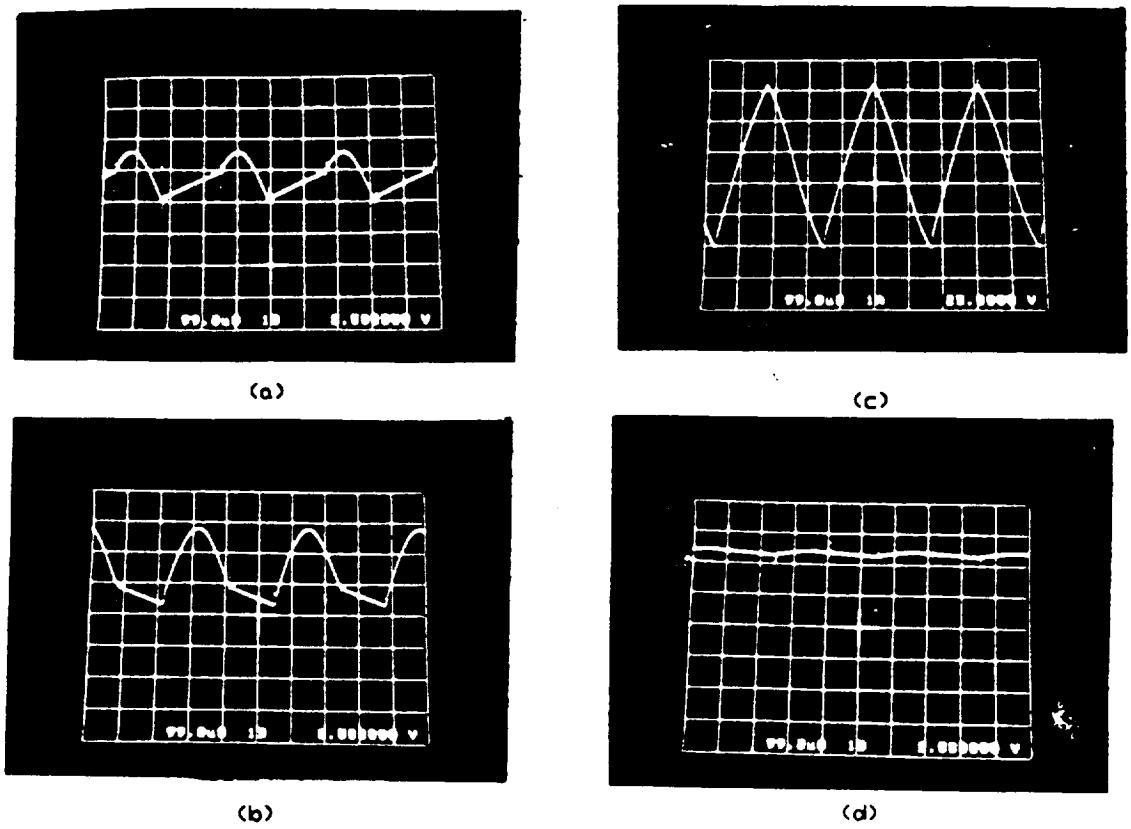


Figure 17. The simulation of the isolated C^3.
From the top, they are coupled capacitor and output voltages, input current, output inductor current and output voltage.



(a) input current, 2.5 A/div.,

(b) output inductor current, 2.5 A/div.,

(c) coupled capacitor voltage, 50 V/div.,

(d) output voltage, 2.5 V/div. Time scale: $100\mu s$.

Oscillograms are taken for $I_1 = 6A$, $I_2 = 4.8A$, and $G = 1.13$.

Figure 18. The experimental results of the C^3.

IV. Low Voltage Inverse Dual Converter

A. Circuit Description

The basic inverse dual converter circuit has been fully investigated and presented in a previous report submitted by this PI to the NASA Johnson Space Center. The inverse dual converter (IDC) [9], which is shown in Figure 19, is also capable of the zero current soft switching and suitable for high power applications due to the elimination of switching losses and the complementary commutation of the switches provided by an ac coupled capacitor. The inherent short circuit and overload protection further improves the reliability of the IDC converter.

For a low voltage aerospace application, such as the NSTS power converter unit (NPCU) in the space station with a nominal 28 VDC output, the basic IDC circuit becomes unrealistic due to the cascaded switch structure. The forward drops of the cascaded switches add up on the circuit path, thus doubling voltage drop and reducing the system efficiency.

However, a low voltage variation of the IDC is presented in Figure 20. This low voltage IDC reduces the cascaded switch numbers at the low voltage output side and minimizes the switching losses with the zero current switching. Only one rectifier switch is connected in series with the dc output at a time in order to decrease the turn-on voltage drops of the switches. The rectifier switches can be replaced by diodes to simplify the control circuit. Moreover, the switches of the full bridge and the rectifier are switched at zero current conditions. Therefore, the efficiency of the low voltage IDC can be increased even at a high switching frequency.

An isolation transformer is also available in this circuit to interface the input source and the dc load, as shown in Figure 21. The coupled capacitor of the basic IDC has been divided into two indentical capacitances, one on the primary and the other on the secondary side of the isolation transformer. These split capacitors can secure the operation of the NPCU system because of the redundancy.

The parasitic leakage inductance of the isolation transformer can be fully utilized in this low voltage IDC circuit with zero current switching. This leakage inductance can be included into the resonant loop with the front end coupled capacitor. During the zero current turn-off process, the leakage inductor can further slow down the decreasing slope of the switch current. This is extremely important for a current mode converter like the IDC to implement with the thyristor switches. Hence, the depth of the reverse recovery charges is dependent on the turn-off slope; the faster the turn-off, the higher the reverse recovery current. The reverse recovery charges cause a circulating current between the main switches even after turning off the switches. This can result in a malfunction of the converter. However, the leakage inductance in this low voltage IDC circuit can reduce the circulating current and also ensure the reliability of the system.

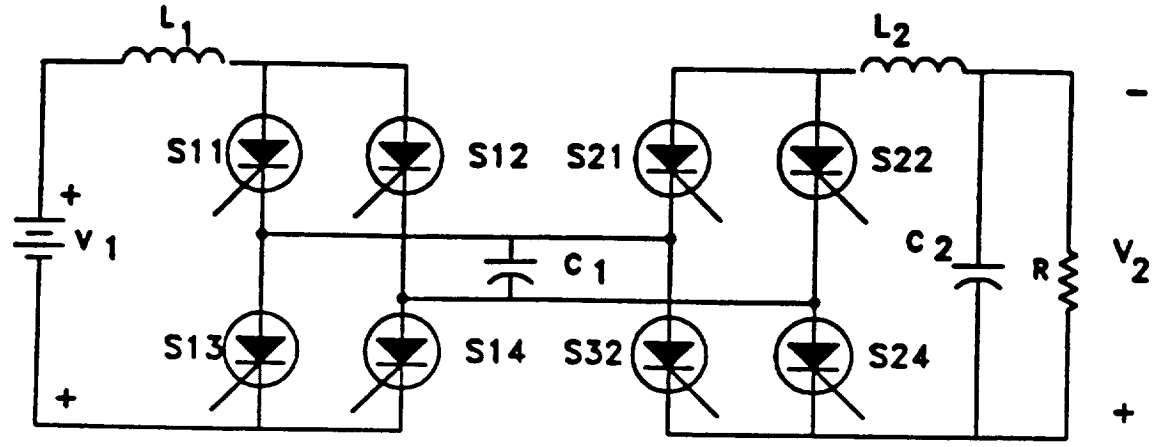


Figure 19. The basic inverse dual converter.

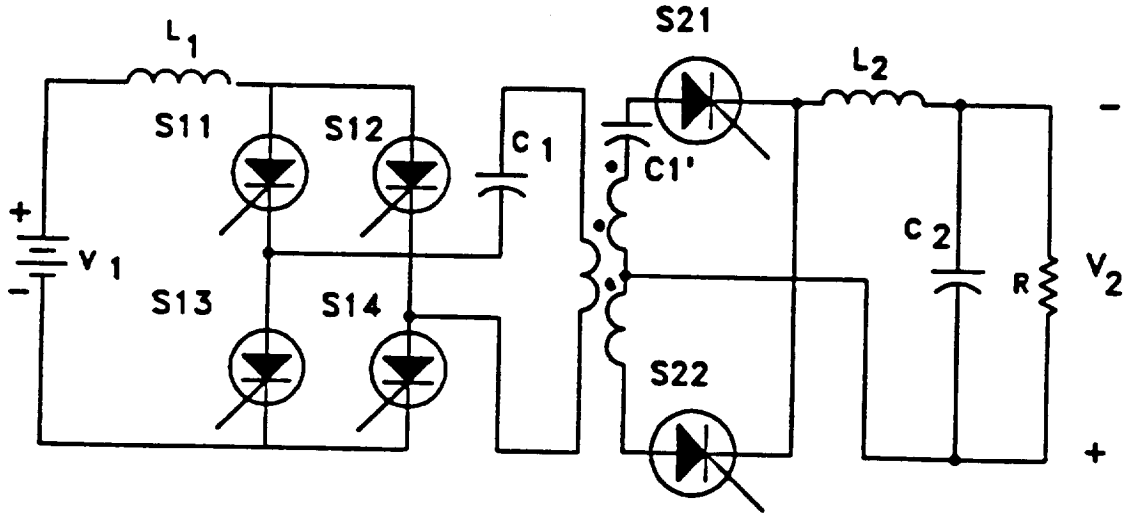


Figure 20. The low voltage IDC.

B. Circuit Operation

The circuit diagram of the low voltage IDC can be simplified as shown in Figure 21. The ac coupled capacitor C is the combination of the two split capacitances and the L_r is the leakage inductance of the isolation transformer. When one switch has to be off, the leakage inductor L_r forms a resonant loop with the coupled capacitor C to shape the current waveform of the switch. By appropriately gating the switches, no additional inductive snubber components are required to guarantee the zero current switching. Hence, this leakage inductor L_r can replace the series inductive snubbers in the zero current switching pair described in the previous chapter and minimize the component numbers.

The switching waveforms of the low voltage IDC are illustrated in Figure 22 and can be divided into 8 different operation stages.

Stage 1. $[t_0, t_1]$: The switches S_1, S_4 and the rectifier diode D_1 turn on at $t = t_0$. The coupled capacitor C is charged and the energy is transferred from the source to the dc load. The leakage inductor L_r is in series with the source inductor L_1 to reduce the input current ripple.

Stage 2. $[t_1, t_2]$: In order to turn off S_4, the switch S_3 should be on at $t = t_1$. A resonant loop is formed through the switches S_3, S_4, the coupled capacitor C, the leakage inductor L_r and the dc output. While S_3 is on with the zero current switching, the resonant current decreases to zero and the switch S_4 turns off at a zero current condition.

Stage 3. $[t_2, t_3]$: The switches S_1 and S_3 are turned on during this interval to charge the source inductor L_1. There is no current flowing through the load

and the capacitor voltage is clamped at V_2.

Stage 4. $[t_3, t_4]$: At $t = t_3$, the switch S_2 turns on. The rectifier diode D_2 is also conducting because of the forward voltage while the switch S_1 is off at a zero current condition due to the resonance between the coupled capacitor C and leakage inductance L_r.

Stage 5. $[t_4, t_5]$: During this interval S_2, S_3 and D_2 are turned on to discharge the coupled capacitor. The source inductor releases the energy stored during $[t_2, t_3]$ to the load.

Stage 6. $[t_5, t_6]$: To repeat the zero current turn off procedure in $[t_1, t_2]$, the switch S_4 is on first in order to turn off S_3 at a zero current condition.

Stage 7. $[t_6, t_7]$: The source inductor L_1 is charged again through the free wheeling operation of the switches S_2 and S_4. The capacitor volatge is then clamped at $-V_2$.

Stage 8. $[t_7, t_8]$: The switch S_1 is turned on at t_7 to switch off S_2 at zero current. The coupled capacitor is charged by the source inductor L_1 to start the next switching cycle.

Note that the switches $S_1 - S_4$ of the low voltage IDC are always switched at zero current conditions to eliminate the switching losses. The rectifier diodes D_1 and D_2 are also turned off with the zero current switching to minimize the reverse recovery current. With the quasi-square current waveforms of the switches, the conduction losses are comparable to the conventional dc-dc converter. Moreover, the voltage imposed on the switches are clamped by the coupled capacitor and are much less than that on the power switch of the zero current switching converter. Normally, the peak voltage of the switch on a

zero current switching converter is two times higher than the input voltage [6]. However, in this low voltage IDC circuit the switch voltage is clamped equal to the dc output and less than the input voltage. Therefore, the voltage as well as the current ratings of the main switches of this low voltage IDC are favorable and the overall system efficiency can be at a higher level.

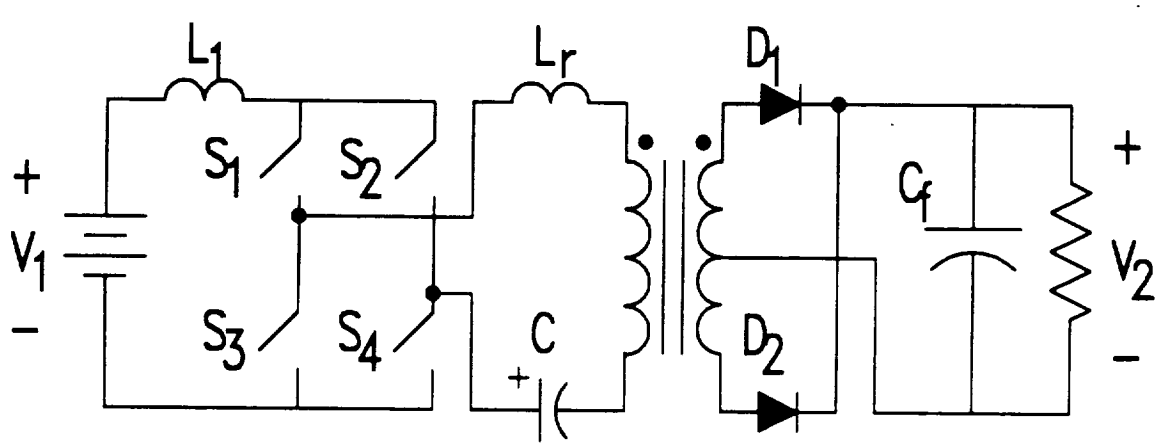


Figure 21. The simplified low voltage IDC.

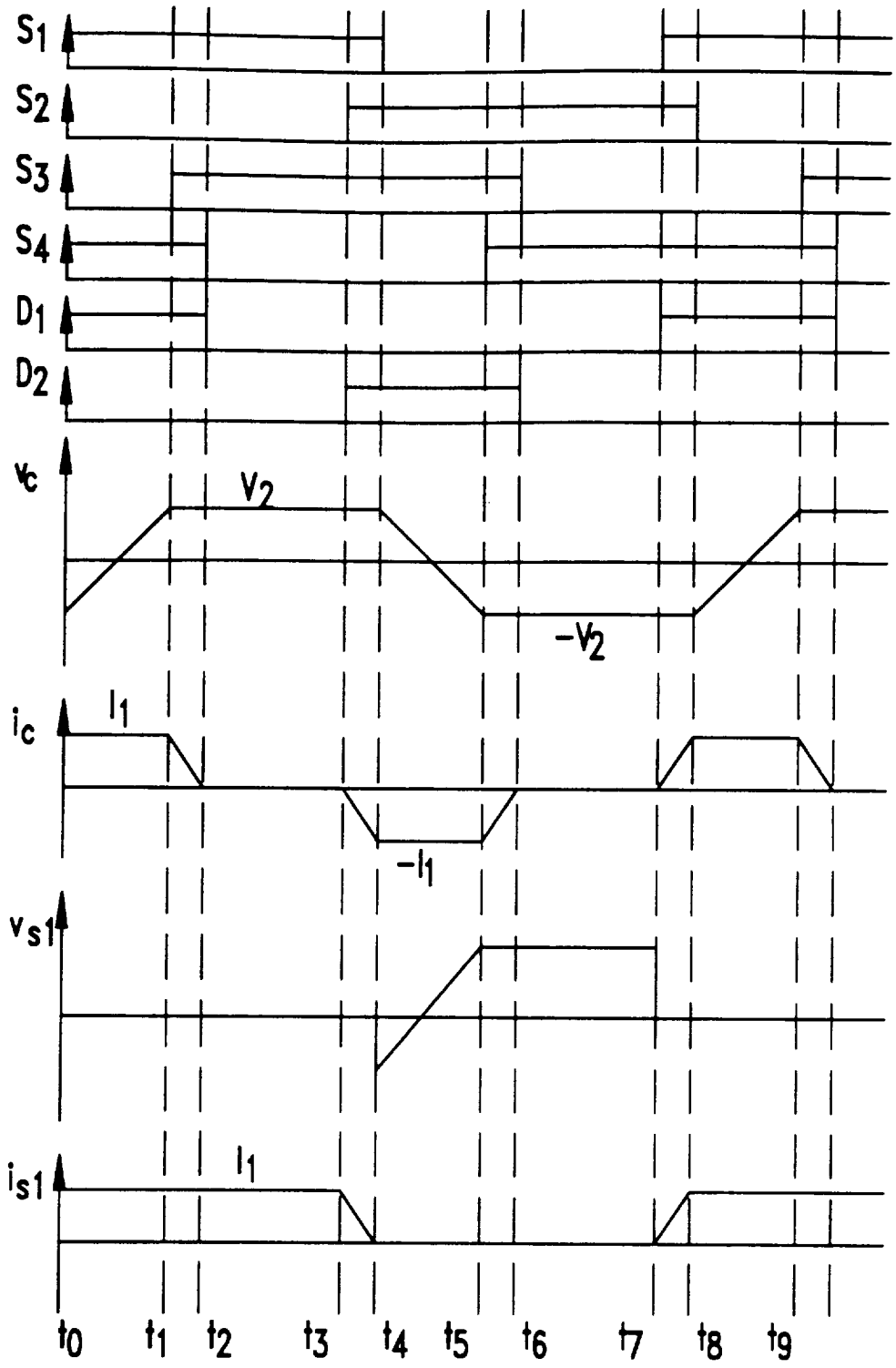


Figure 22. The waveforms of the low voltage IDC.

C. Circuit Analysis

Assume continous conduction in the source inductor L_1 and negligible resonant period when the low voltage IDC is operating in the steady state. Let D denotes the charging duration of the source inductor. Hence, the inductive energy stored during the charging time should be totally transferred to the dc load over one cycle. The following volt-sec balance equation must be satisfied according to the waveforms shown in Figure 23.

$$\int_0^{T/2} v_{L1}(t)dt = 0$$

where T is the switching period of this converter. The dc voltage gain can be determined from the above equation.

$$\frac{V_2}{V_1} = \frac{D}{1-D} \tag{1}$$

The dc output voltage can be controlled by the duty cycle of the charging time of the source inductor L_1. Therefore, the low voltage IDC circuit can operate with zero current switching, while controlled by pulse width modulation (PWM) technique. As far as the NPCU system is concerned, this gain function should be set to 0.175 with a 160 VDC input and 28 VDC output. The charging cycle of the source inductor can then be given by $D = 0.149$.

The rising time t_{rv} of the capacitor voltage is dependent on the charging current I_1 and the capacitance C.

$$
\begin{aligned}
t_{rv} &= \frac{C\Delta v_c}{I_1} \\
&= \frac{2CV_2}{I_1}
\end{aligned}
\tag{2}
$$

However, the rising time t_{rv} is equal to the discharging cycle of the source inductor such that $t_{rv} = (1 - D)T/2$, where T is the switching period of the main switches. Therefore, the switching frequency can be found as follows.

$$
f_s = \frac{(1 - D)I_1}{4CV_2} \tag{3}
$$

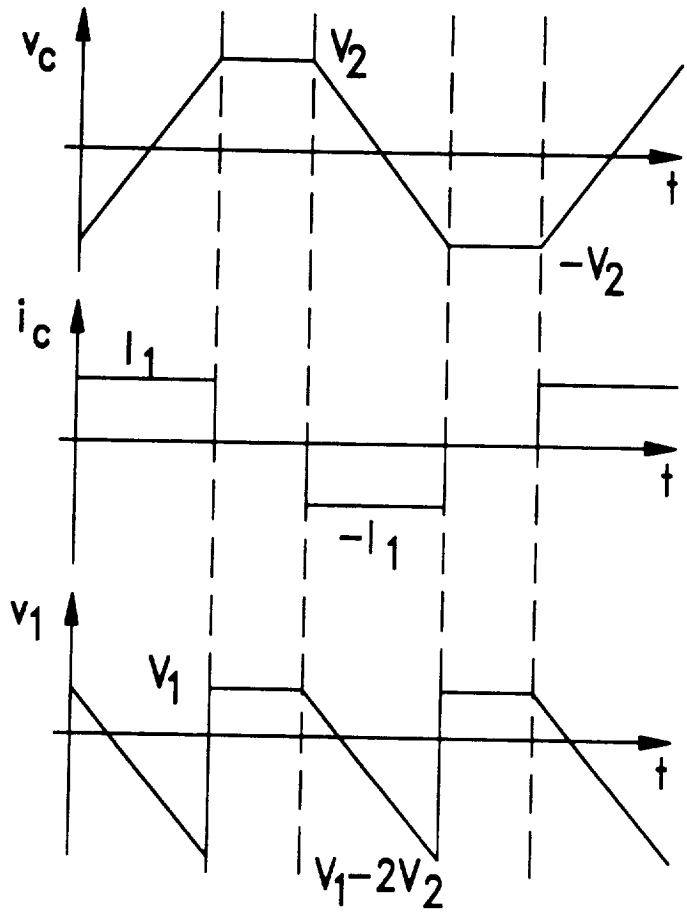


Figure 23. The steady state waveforms.

D. Efficiency Calculation

The specifications of the NPCU system are given as follows.

Input voltage,	$V_1 = 160$ VDC
Output voltage,	$V_2 = 28$ VDC
Output power,	$P_d = 2.5$ KW for each cell.
DC gain,	$G = 0.175$

If the low voltage IDC is used for the NPCU system and assumes that the turns ratio of the isolation transformer is 1 : 1, the input and output currents can be caculated as $I_1 = 15.63A$ and $I_2 = 89.29A$ respectively. The number of the cascaded switches in the full bridge is always 2 while only one diode of the rectifier is on at a time during the operation. The rectifier diodes are conducting only when the coupled capacitor is charged or discharged. Supposing the on-state voltage drop of the switch and diode is $1V$, the average conduction losses for the full bridge and the rectifier can be found from the following caculations.

$$P_{FB} = 15.63A \times 1V \times 2 = 31.26W$$

$$P_{rect.} = 15.63A \times 1V \times (1 - 0.149) = 13.3W$$

The total average conduction loss is

$$\begin{aligned} P_{cond.} &= P_{Fb} + P_{rect.} \\ &= 44.56W. \end{aligned}$$

The theoretical system efficiency can be determined as follows.

$$\eta = (1 - \frac{P_{cond.}}{P_{in}}) \times 100\%$$

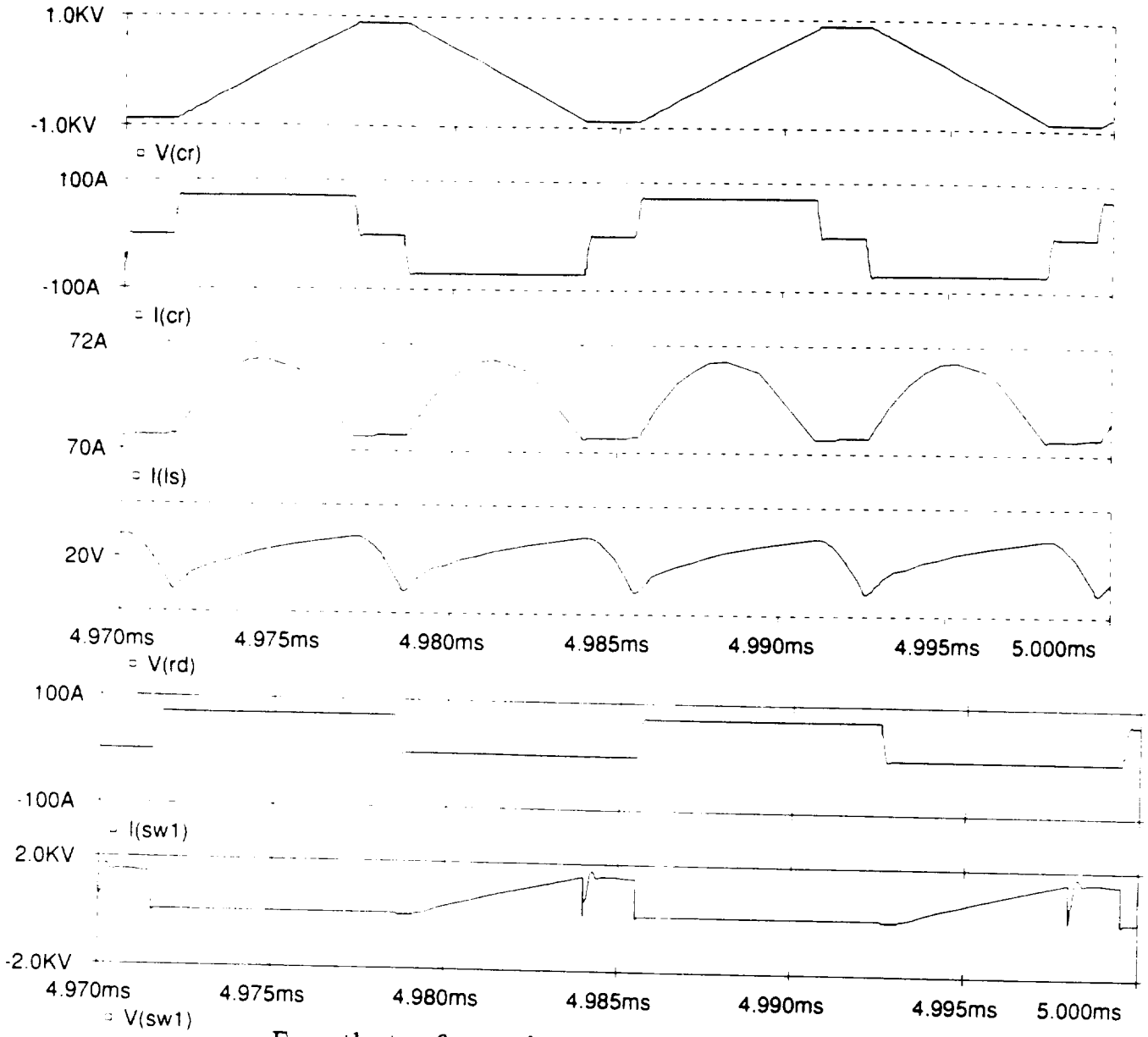
$$= (1 - \frac{44.56}{2500}) \times 100\%$$

$$= 98\%$$

The actual efficiency of the low voltage IDC will be lower because of the stray losses on the components and the copper and eddy losses of the isolation transformer.

F. Simulation Results

Figure 24 shows the simulations of the low voltage IDC circuit.



From the top figure, they are coupled capacitor voltage, capacitor current, input current, output voltage, switch current and voltage, respectively.

Figure 24. The simulation results of the low voltage IDC.

V. Conclusions

The study of the soft swtiching dc-dc converter at Texas A&M University Power Electronics Laboratory for the space station power exchange units has resulted in the discovery of a new family of zero current switching dc-dc converters. Four related papers have been published last year. The isolated C^3 and the low voltage IDC, which belong to this new zero current switching family, are proposed for the APCU and NPCU systems.

With the elimination of the switching losses and a higher system efficiency due to the zero current switching operation, the isolated C^3 is shown to be capable of step-up and step-down the output voltage by controlling the magnitude of the coupled capacitor and is particularly suitable for both the APCU and NPCU applications. The research of this isolated C^3 has been focused on the theoretical analysis, simulation and a prototype of this converter circuit.

The low voltage IDC is designed for the NPCU system because only one switch is connected in series with the low voltage output at a time in order to reduce the on-state voltage drops. The low voltage IDC is derived from the zero current switching buck type converter and can transform 160 VDC input to the 28 VDC output with high efficiency. At the present development of the low voltage IDC has been the numerical analysis and simulations. The future objectives are expected to be dynamic control of the low voltage IDC and a prototype circuit for illustration.

Meanwhile, an ac version of the above new zero current switching converters has been invented and may be possible for the space shuttle actuator or hydraulic pump drive applications. The present objectives of this project are to further study these isolated ZCS dc-dc converters for the space power ex-

change units and the dc-ac variation, for space shuttle actuator and hydraulic pump drives.

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